# LOW VOLTAGE 4 Megabit (512K x 8) OTP EPROM

**PRELIMINARY DATA**

- PIN COMPATIBLE with the 4 MEGABIT, SINGLE VOLTAGE FLASH MEMORY
- LOW VOLTAGE READ OPERATION: 3V to 5.5V
- FAST ACCESS TIME: 120ns
- LOW POWER ”CMOS” CONSUMPTION:
  – Active Current 15mA
  – Standby Current 20µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES:
  – Typical 48sec. (PRESTO II Algorithm)
  – Typical 27sec. (On-Board Programming)
- M27V405 is PROGRAMMABLE as M27C405 with IDENTICAL SIGNATURE

PLCC32 (K)

TSOP32 (N)
8 x 20mm

## DESCRIPTION

The M27V405 is a low voltage, low power 4 Megabit One Time Programmable EPROM, organised as 524,288 by 8 bits. It is ideally suited for microprocessor systems requiring large programs, in the application where the contents is stable and needs to be programmed only one time.

The M27V405 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

**Figure 1. Logic Diagram**

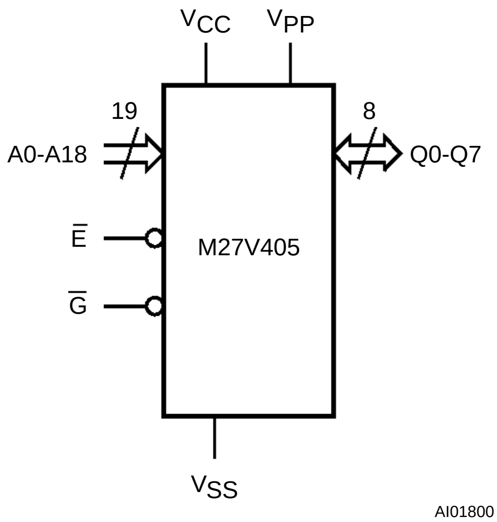



**Table 1. Signal Names**

| | |
|---|---|
| A0 - A18 | Address Inputs |
| Q0 - Q7 | Data Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $V_{PP}$ | Program Supply |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 2A. LCC Pin Connections**

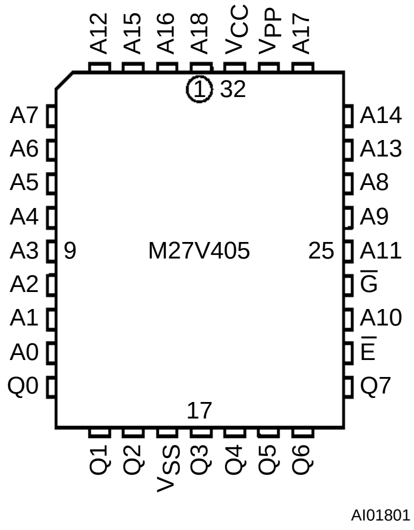



**Figure 2B. TSOP Pin Connections**

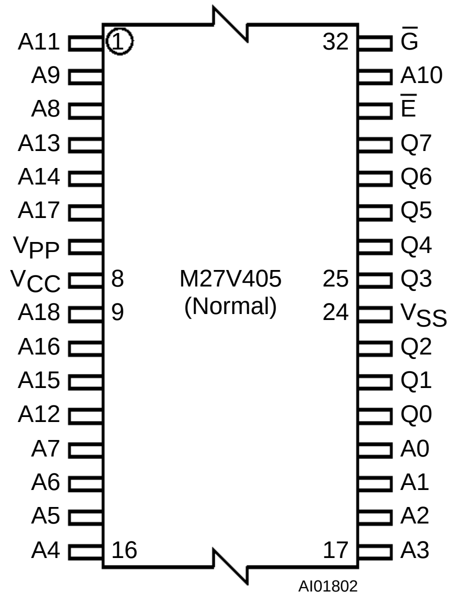



**Table 2. Absolute Maximum Ratings (1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | –40 to 125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –50 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{IO}$ (2) | Input or Output Voltages (except A9) | –2 to 7 | V |
| $V_{CC}$ | Supply Voltage | –2 to 7 | V |
| $V_{A9}$ (2) | A9 Voltage | –2 to 13.5 | V |
| $V_{PP}$ | Program Supply Voltage | –2 to 14 | V |

**Notes:** 1. Except for the rating ”Operating Temperature Range”, stresses above those listed in the Table ”Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is $V_{CC}$ +0.5V with possible overshoot to $V_{CC}$ +2V for a period less than 20ns.

**DESCRIPTION** (cont’d)

The M27V405 is pin compatible with the industry standard 4 Megabit, single voltage FLASH Memory. It can be considered as a FLASH Low Cost solution for production quantities.

The M27V405 can also be operated as a standard 4 Megabit OTP EPROM (similar to M27C405) with a 5V power supply. The M27V405 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

## DEVICE OPERATION

The modes of operations of the M27V405 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for $V_{pp}$ and 12V on A9 for Electronic Signature.

### Read Mode

The M27V405 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time ($t_{AVQV}$) is equal to the delay from $\overline{E}$ to output ($t_{ELQV}$). Data is available at the output after a delay of $t_{GLQV}$ from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least $t_{AVQV}$-$t_{GLQV}$.

### Standby Mode

The M27V405 has a standby mode which reduces the active current from 15mA to 20µA with low voltage operation $V_{CC} \leq 3.3V$ (30mA to 100µA with a supply of 5.5V), see Read Mode DC Characteristics Table for details. The M27V405 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

### Two Line Output Control

Because OTP EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

### System Considerations

The power switching characteristics of Advanced CMOS OTP EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The

**Table 3. Operating Modes**

| Mode | $\overline{E}$ | $\overline{G}$ | A9 | $V_{PP}$ | Q0 - Q7 |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | X | $V_{CC}$ or $V_{SS}$ | Data Out |
| Output Disable | $V_{IL}$ | $V_{IH}$ | X | $V_{CC}$ or $V_{SS}$ | Hi-Z |
| Program | $V_{IL}$ Pulse | $V_{IH}$ | X | $V_{PP}$ | Data In |
| Verify | $V_{IH}$ | $V_{IL}$ | X | $V_{PP}$ | Data Out |
| Program Inhibit | $V_{IH}$ | $V_{IH}$ | X | $V_{PP}$ | Hi-Z |
| Standby | $V_{IH}$ | X | X | $V_{CC}$ or $V_{SS}$ | Hi-Z |
| Electronic Signature | $V_{IL}$ | $V_{IL}$ | $V_{ID}$ | $V_{CC}$ | Codes |

**Note**: X = $V_{IH}$ or $V_{IL}$, $V_{ID}$ = 12V ± 0.5V

**Table 4. Electronic Signature**

| Identifier | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer's Code | $V_{IL}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device Code | $V_{IH}$ | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4h |

**Table 5. AC Measurement Conditions**

| | High Speed | Standard |
|---|---|---|
| Input Rise and Fall Times | ≤ 10ns | ≤ 20ns |
| Input Pulse Voltages | 0 to 3V | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V | 0.8V and 2V |

**Figure 3. AC Testing Input Output Waveform**

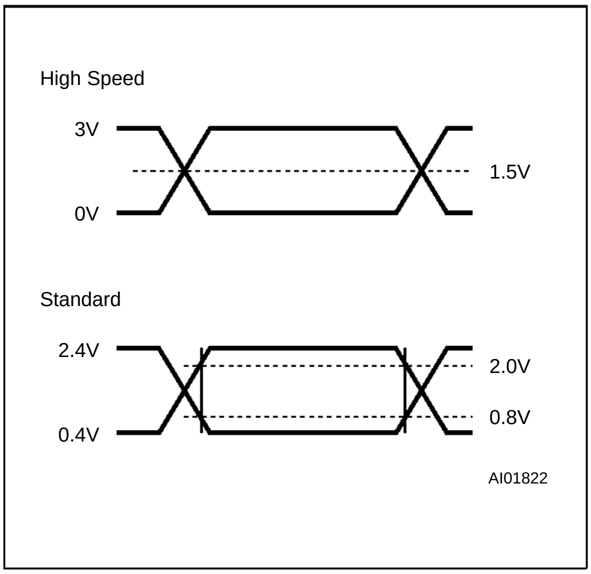



**Figure 4. AC Testing Load Circuit**

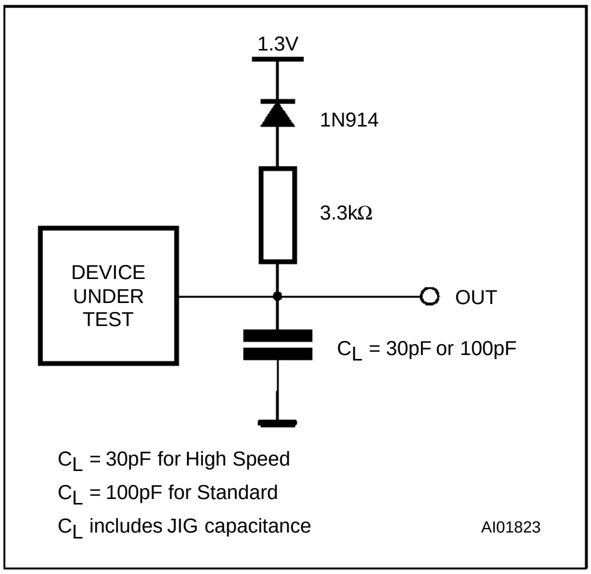



**Table 6. Capacitance** (1) ($T_A$ = 25 °C, f = 1 MHz )

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 12 | pF |

**Note:** 1. Sampled only, not 100% tested.

**DEVICE OPERATION** (cont'd)

magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between $V_{CC}$ and $V_{SS}$. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between $V_{CC}$ and $V_{SS}$ for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Programming**

When delivered, all bits of the M27V405 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The M27V405 is in the programming mode when $V_{PP}$ input is at 12.75V, $\overline{G}$ is at $V_{IH}$ and $\overline{E}$ is pulsed to $V_{IL}$.

### Table 7. Read Mode DC Characteristics (1)
($T_A$ = 0 to 70°C, –20 to 70°C, –20 to 85°C or –40 to 85°C; $V_{CC}$ = 3.3V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | | ±10 | µA |
| $I_{LO}$ | Output Leakage Current | 0V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | ±10 | µA |
| $I_{CC}$ | Supply Current | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$, $I_{OUT}$ = 0mA, f = 5MHz, $V_{CC}$ = 3.2V | | 15 | mA |
| | | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$, $I_{OUT}$ = 0mA, f = 5MHz, $V_{CC}$ = 5.5V | | 30 | mA |
| $I_{CC1}$ | Supply Current (Standby) TTL | $\overline{E}$ = $V_{IH}$ | | 1 | mA |
| $I_{CC2}$ | Supply Current (Standby) CMOS | $\overline{E}$ > $V_{CC}$ – 0.2V, $V_{CC}$ = 3.2V | | 20 | µA |
| | | $\overline{E}$ > $V_{CC}$ – 0.2V, $V_{CC}$ = 5.5V | | 100 | µA |
| $I_{PP}$ | Program Current | $V_{PP}$ = $V_{CC}$ | | 10 | µA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ (2) | Input High Voltage | | 2 | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –400µA | 2.4 | | V |
| | Output High Voltage CMOS | $I_{OH}$ = –100µA | $V_{CC}$ – 0.7V | | V |

**Notes:** 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Maximum DC voltage on Output is $V_{CC}$ +0.5V.

### Table 8A. Read Mode AC Characteristics (1)
($T_A$ = 0 to 70°C, –20 to 70°C, –20 to 85°C or –40 to 85°C; $V_{CC}$ = 3.3V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27V405 | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | -120 (3) | | -150 | | |
| | | | | Min | Max | Min | Max | |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | | 120 | | 150 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G}$ = $V_{IL}$ | | 120 | | 150 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E}$ = $V_{IL}$ | | 60 | | 80 | ns |
| $t_{EHQZ}$ (2) | $t_{DF}$ | Chip Enable High to Output Hi-Z | $\overline{G}$ = $V_{IL}$ | 0 | 50 | 0 | 50 | ns |
| $t_{GHQZ}$ (2) | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E}$ = $V_{IL}$ | 0 | 50 | 0 | 50 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | 0 | | 0 | | ns |

**Notes:** 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.
3. In case of 120ns speed see High Speed AC Measurement conditions.

**Table 8B. Read Mode AC Characteristics** [(1)]
($T_A$ = 0 to 70°C, –20 to 70°C, –20 to 85°C or –40 to 85°C; $V_{CC}$ = 3.3V ± 10%; $V_{PP}$ = $V_{CC}$)

| Symbol | Alt | Parameter | Test Condition | M27V405 | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | -180 | | -200 | | |
| | | | | Min | Max | Min | Max | |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | | 180 | | 200 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G} = V_{IL}$ | | 180 | | 200 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E} = V_{IL}$ | | 90 | | 100 | ns |
| $t_{EHQZ}$ [(2)] | $t_{DF}$ | Chip Enable High to Output Hi-Z | $\overline{G} = V_{IL}$ | 0 | 50 | 0 | 70 | ns |
| $t_{GHQZ}$ [(2)] | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E} = V_{IL}$ | 0 | 50 | 0 | 70 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Address Transition to Output Transition | $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$ | 0 | | 0 | | ns |

**Notes:** 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.

**Figure 5. Read Mode AC Waveforms**

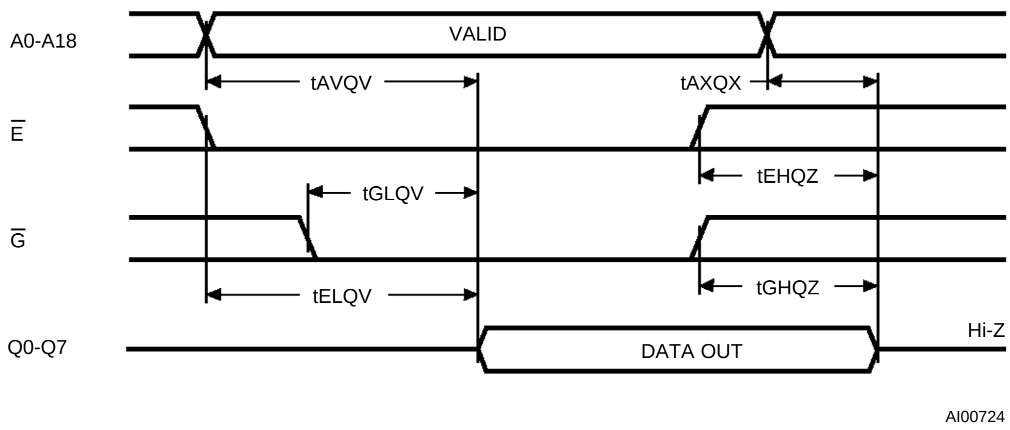


**Table 9. Programming Mode DC Characteristics (1)**
($T_A$ = 25 °C; $V_{CC}$ = 6.25V ± 0.25V; $V_{PP}$ = 12.75V ± 0.25V)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0 \le V_{IN} \le V_{CC}$ | | ±10 | µA |
| $I_{CC}$ | Supply Current | | | 50 | mA |
| $I_{PP}$ | Program Current | $\overline{E} = V_{IL}$ | | 50 | mA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –400µA | 2.4 | | V |
| $V_{ID}$ | A9 Voltage | | 11.5 | 12.5 | V |

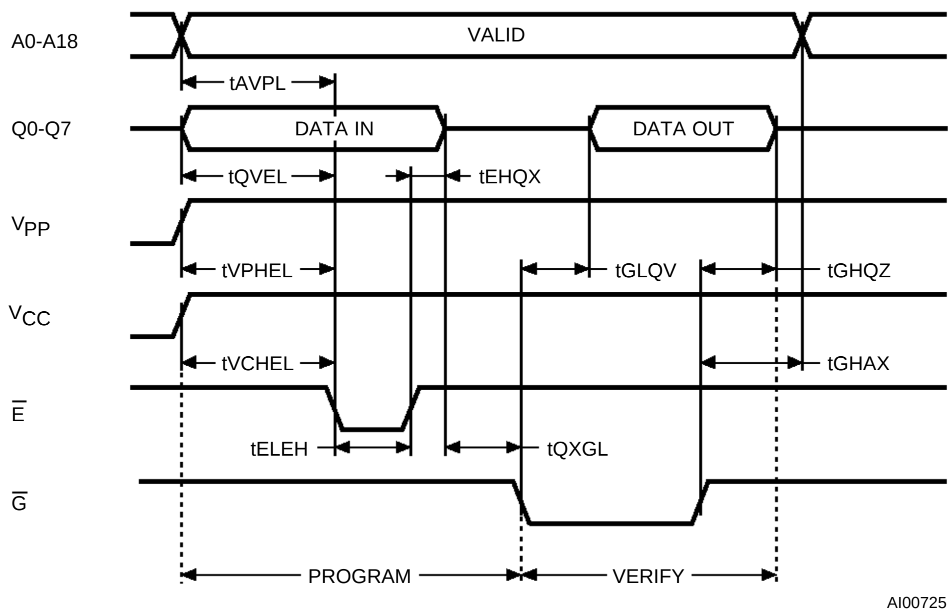
**Note:** 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.

**Table 10. Programming Mode AC Characteristics (1)**
($T_A$ = 25 °C; $V_{CC}$ = 6.25V ± 0.25V; $V_{PP}$ = 12.75V ± 0.25V)

| Symbol | Alt | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{AVEL}$ | $t_{AS}$ | Address Valid to Chip Enable Low | | 2 | | µs |
| $t_{QVEL}$ | $t_{DS}$ | Input Valid to Chip Enable Low | | 2 | | µs |
| $t_{VPHEL}$ | $t_{VPS}$ | $V_{PP}$ High to Chip Enable Low | | 2 | | µs |
| $t_{VCHEL}$ | $t_{VCS}$ | $V_{CC}$ High to Chip Enable Low | | 2 | | µs |
| $t_{ELEH}$ | $t_{PW}$ | Chip Enable Program Pulse Width | | 95 | 105 | µs |
| $t_{EHQX}$ | $t_{DH}$ | Chip Enable High to Input Transition | | 2 | | µs |
| $t_{QXGL}$ | $t_{OES}$ | Input Transition to Output Enable Low | | 2 | | µs |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | | | 100 | ns |
| $t_{GHQZ}$ | $t_{DFP}$ | Output Enable High to Output Hi-Z | | 0 | 130 | ns |
| $t_{GHAX}$ | $t_{AH}$ | Output Enable High to Address Transition | | 0 | | ns |

**Notes:** 1. $V_{CC}$ must be applied simultaneously with or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Sampled only, not 100% tested.

**Figure 6. Programming and Verify Modes AC Waveforms**




**DEVICE OPERATION** (cont'd)

The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. $V_{CC}$ is specified to be 6.25V ± 0.25V, but it can be set to lower values in case of On-Board Programming (see dedicated paragraph).

**PRESTO II Programming Algorithm**

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. Programming with PRESTO II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs (see Figure 7). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

**Program Inhibit**

Programming of multiple M27V405s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27V405 may be common. A TTL low level pulse applied to a M27V405's $\overline{E}$ input, with $V_{PP}$ at 12.75V, will program that M27V405. A high level $\overline{E}$ input inhibits the other M27V405s from being programmed.

**Program Verify**

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at $V_{IL}$ , $\overline{E}$ at $V_{IH}$, $V_{PP}$ at 12.75V and $V_{CC}$ at 6.25V.

**On-Board Programming**

Programming the M27V405 may be performed directly in the application circuit, however this requires modification to the PRESTO II Algorithm (see Figure 8). For in-circuit programming $V_{CC}$ is determined by the user and normally is compatible with other components using the same supply voltage. It is recommended that the maximum value of $V_{CC}$ which remains compatible with the circuit is used.

Typically $V_{CC}$=5.5V for programming systems using $V_{CC}$=5V, and $V_{CC}$=3.5V for low voltage 3V systems is recommended. The value of $V_{CC}$ does not affect the programming, it gives a higher test capability in VERIFY mode.

$V_{PP}$ must be kept at 12.75 volts to maintain and enable the programming.

**Figure 7. Programming Flowchart**

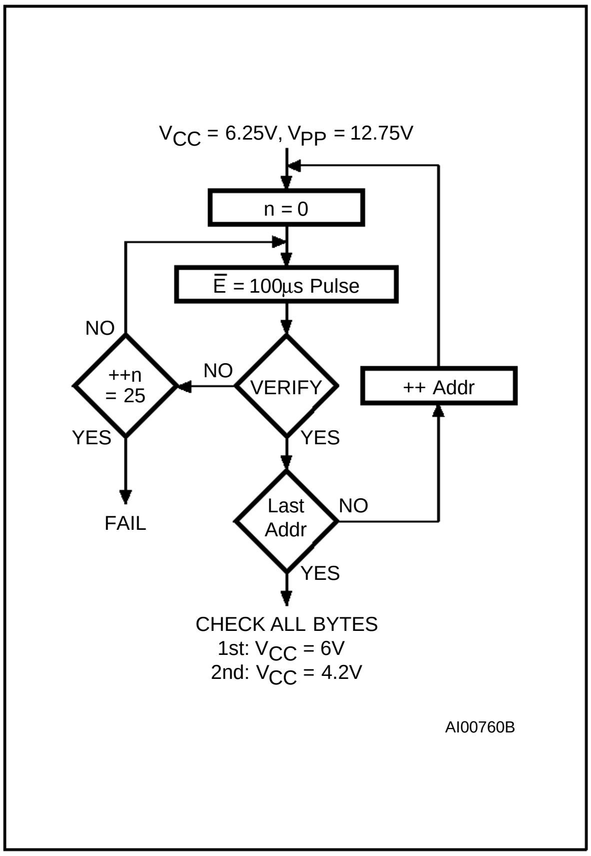
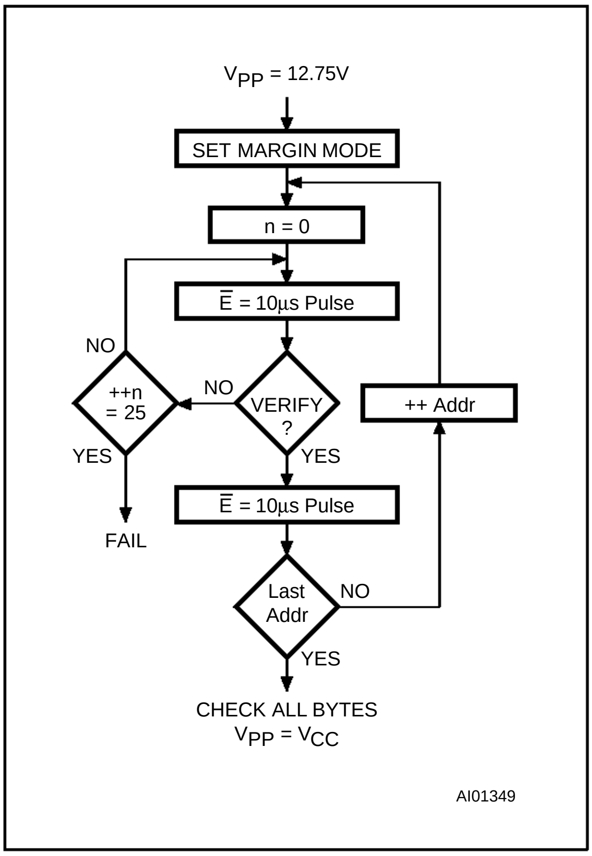



**Figure 8. On-Board Programming Flowchart**




**Warning: compatibility with FLASH Memory**

Compatibility issues may arise when replacing the compatible Single Supply 4 Megabit FLASH Memory (the M29F040) by the M27V405.

The $V_{PP}$ pin of the M27V405 corresponds to the "W" pin of the M29F040. The M27V405 $V_{PP}$ pin can withstand voltages up to 12.75V, while the "W" pin of the M29F040 is a normal control signal input and may be damaged if a high voltage is applied; special precautions must be taken when programming in-circuit.

However if an already programmed M27V405 is used, this can be directly put in place of the FLASH Memory as the $V_{PP}$ input, when not in programming mode, is set to $V_{CC}$ or $V_{SS}$.

***Changes to PRESTO II.*** The duration of the programming pulse is reduced to 20µs, making the programming time of the M27V405 comparable with the counterpart FLASH Memory.

**Electronic Signature**

The Electronic Signature (ES) mode allows the reading out of a binary code from an OTP EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27V405. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V405 with $V_{PP}$=$V_{CC}$=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during Electronic Signature mode. Byte 0 (A0=$V_{IL}$) represents the manufacturer code and byte 1 (A0=$V_{IH}$) the device identifier code. For the SGS-THOMSON M27V405, these two identifier bytes are given in Table 4 and can be read-out on outputs Q0 to Q7.

## ORDERING INFORMATION SCHEME

Example: M27V405 -150 K 1 TR

| Speed | | Package | | Temperature Range | | Option | |
|---|---|---|---|---|---|---|---|
| -120 [1] | 120 ns | K | PLCC32 | 1 | 0 to 70 °C | TR | Tape & Reel Packing |
| -150 | 150 ns | N | TSOP32 8 x 20mm | 4 | –20 to 70 °C | | |
| -180 | 180 ns | | | 5 | –20 to 85 °C | | |
| -200 | 200 ns | | | 6 | –40 to 85 °C | | |

**Note:** 1. High Speed, see AC Characteristics section for further information.

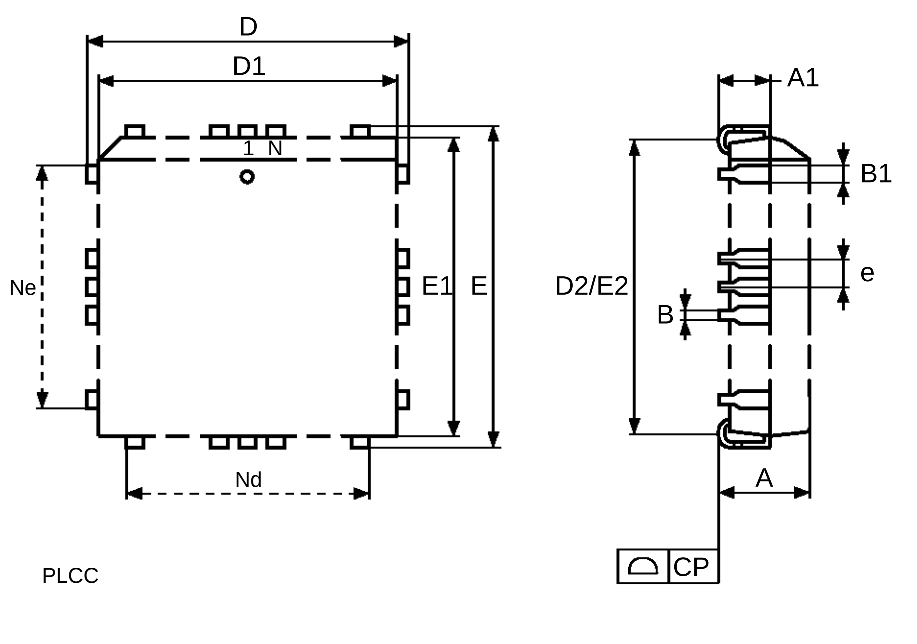
For a list of available options (Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

## PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 2.54 | 3.56 | | 0.100 | 0.140 |
| A1 | | 1.52 | 2.41 | | 0.060 | 0.095 |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| D | | 12.32 | 12.57 | | 0.485 | 0.495 |
| D1 | | 11.35 | 11.56 | | 0.447 | 0.455 |
| D2 | | 9.91 | 10.92 | | 0.390 | 0.430 |
| E | | 14.86 | 15.11 | | 0.585 | 0.595 |
| E1 | | 13.89 | 14.10 | | 0.547 | 0.555 |
| E2 | | 12.45 | 13.46 | | 0.490 | 0.530 |
| e | 1.27 | – | – | 0.050 | – | – |
| N | 32 | | | 32 | | |
| Nd | 7 | | | 7 | | |
| Ne | 9 | | | 9 | | |
| CP | | | 0.10 | | | 0.004 |

PLCC32

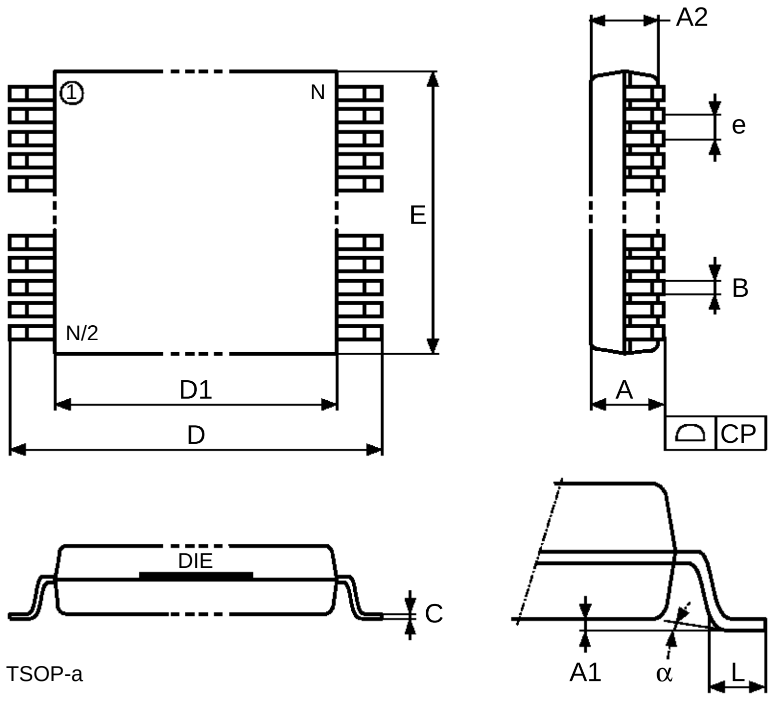



Drawing is not to scale.

## TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.05 | 0.17 | | 0.002 | 0.006 |
| A2 | | 0.95 | 1.50 | | 0.037 | 0.059 |
| B | | 0.15 | 0.27 | | 0.006 | 0.011 |
| C | | 0.10 | 0.21 | | 0.004 | 0.008 |
| D | | 19.80 | 20.20 | | 0.780 | 0.795 |
| D1 | | 18.30 | 18.50 | | 0.720 | 0.728 |
| E | | 7.90 | 8.10 | | 0.311 | 0.319 |
| e | 0.50 | – | – | 0.020 | – | – |
| L | | 0.50 | 0.70 | | 0.020 | 0.028 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |
| CP | | | 0.10 | | | 0.004 |

TSOP32




TSOP-a

Drawing is not to scale.